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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,611	09/12/2003	Chun Ho Fan	50626.55	6110

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,611	FAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,15-23,25 and 26* is/are pending in the application.

4a) Of the above claim(s) *18,19 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,15-17,20-23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicants' arguments filed on August 14, 2006 found persuasive and the application is reopened as indicated on the Notice of the Panel Decision from Pre-Appeal Brief Review. However, upon further consideration, a new ground(s) of rejection is made in view Melton et al. (US 6,194,250) and Futakuchi (US 6,308,938).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 13, 15- 17, 20-23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Futakuchi (US 6,308,938) in view of Melton et al. (US 6,194,250).

Re claim 13, Futakuchi discloses an integrated circuit package comprising: a substrate (3) (see Fig. 10) having a plurality of conductive traces (7) (i.e., bonding wire **7** as commonly known as conductive trace); a semiconductor die (1) mounted to the substrate such that bumps (12) of said semiconductor die (1) (see Fig. 10) are electrically connected to the plurality of conductive traces (7) of the substrate (3); an overmold material (5) encapsulating said semiconductor die (1) and a ball grid array (8) disposed on a second surface of the substrate (3) and in electrical connection with conductive traces (7) (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25).

However, Futakuchi does not disclose a plurality of balls disposed on a first surface of said substrate; said balls on said substrate such that portions of said balls that are disposed farthest from said substrate are exposed at an exterior of said integrated circuit package.

Melton et al. disclose an integrated circuit packaging comprising a support (i.e., a substrate) (38) having a plurality of conductive traces (18); a plurality of balls (20) (i.e., metallic bumps) disposed on a first surface of the substrate (38) (see Fig. 4); a semiconductor die (12) mounted to the substrate (38) such that bumps (20) of the semiconductor die (12) are electrically connected to said plurality of conductive traces (18) of the substrate (38); an overmold material (34) encapsulating the semiconductor die (12) and the balls (20) on the substrate (38) such that portions of said balls (20) that are disposed farthest from the substrate (38) are exposed at an exterior of the integrated circuit package (see Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

As Melton et al. disclose that "the resulting polymeric body 14 encapsulates active face **28** of integrated circuit die **12**, the plurality of wire leads 18, inner surface 19, and metallic

bumps **20**, thereby protecting them from environmental exposure and damage experienced during normal use of microelectronic package **10.** Second surface **26** is formed opposite first surface **24** by the surface tension of the polymeric precursor. In a preferred embodiment, first surface 24, non-active face **32**, and outer surface 17 cooperate to form planar surface 37. Planar surface 37 facilitates the manipulation of microelectronic assembly **10** by conventional robotic end effectors having vacuum pickup ends or the like. Bonding surface **30** of each metallic bump **20** is exposed at second surface **26** of polymeric body **14** and protrudes from second surface **26** to provide a surface capable of forming reliable solder interconnections. The exposure of bonding surface **30** provides a bonding surface that is able to be attached to solder bumps or bond pads on a printed circuit board or the like." (See Melton et al. Col. 4, lines 36-55).

Both Futakuchi '938 and Melton et al. '250 teachings are directed to semiconductor device package the package includes the ball grid array and over mold resin. Therefore, the teachings of Futakuchi '938 and Melton et al. '250 are analogous. Hence, one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful structure a plurality of balls disposed on a first surface of said substrate; said balls on said substrate such that portions of said balls that are disposed farthest from said substrate are exposed at an exterior of said integrated circuit package as disclosed by Melton et al. '250 in order to provide a surface capable of forming reliable solder interconnections and the exposure of bonding surface provides a bonding surface that is able to be attached to solder bumps or bond pads on a printed circuit board or the like.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Futakuchi reference with a plurality of balls disposed on a first surface of said substrate; said balls on said substrate such that portions of said balls that are disposed farthest from said substrate are exposed at an exterior of said integrated circuit package as taught by Melton et al. in order to provide a surface capable of forming reliable solder interconnections and the exposure of bonding surface provides a bonding surface that is able to be attached to solder bumps or bond pads on a printed circuit board or the like.

Re claim 15, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including wherein said plurality of balls is attached to respective solder ball pads on said first surface of said substrate.

Re claim 16, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including wherein said bumps of said semiconductor die are electrically connected to the conductive traces by wire bonds (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25 and Melton et al. Col. 4, lines 36-55).

Re claim 17, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including wherein said semiconductor die is fixed to said first surface of said substrate (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25 and Melton et al. Col. 4, lines 36-55).

Re claim 20, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including wherein said plurality of balls circumscribe said

semiconductor die (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25 and Melton et al. Col. 4, lines 36-55).

Re claim 21, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including wherein said plurality of balls is electrically connected to said conductive traces of said substrate (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25 and Melton et al. Col. 4, lines 36-55).

Re claim 22, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including wherein said balls are deformed (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25 and Melton et al. Col. 4, lines 36-55).

Re claim 23, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including a die adapter mounted on said semiconductor die and encapsulated in said overmold material (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25 and Melton et al. Col. 4, lines 36-55).

Re claim 25, as applied to claim 13 above, Futakuchi and Melton et al. in combination disclose all the claimed limitations including wherein said plurality of balls is comprised of a plurality of solder balls (see Futakuchi Fig. 10 and related text in Col. 1, line 35-Col. 2, line 25 and Melton et al. Col. 4, lines 36-55).

Response to Arguments

4. Applicants' arguments with respect to claims 13, 15- 17, 20-23, and 25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brook Kebede
Primary Examiner
Art Unit 2823

BK
November 13, 2006